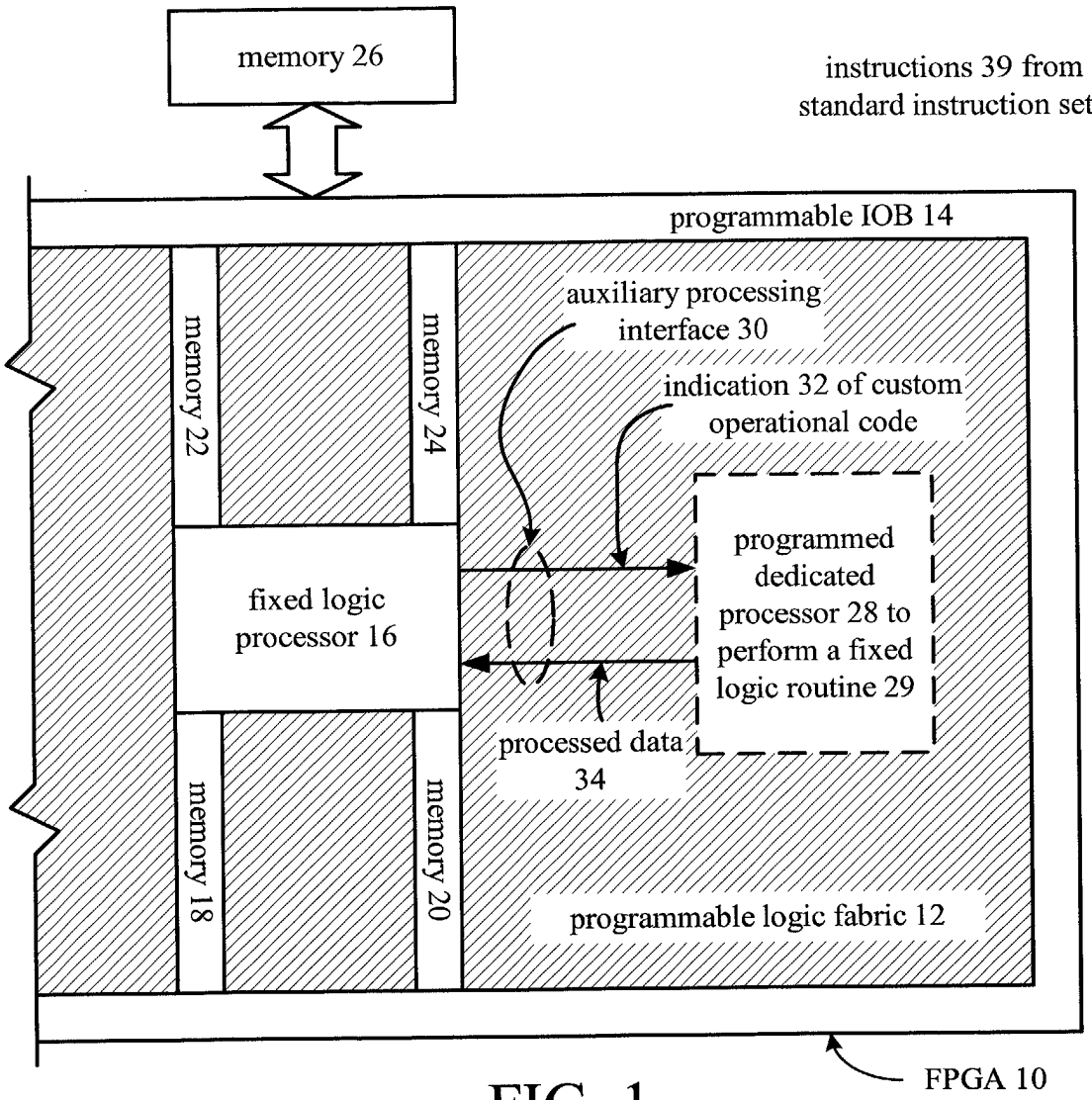
memory 26
programmable IOB 14
memory 22
memory 24
auxiliary processing interface 30
indication 32 of custom operational code
fixed logic processor 16
programmed dedicated processor 28 to perform a fixed logic routine 29
processed data 34
memory 18
memory 20
programmable logic fabric 12
FPGA 10

FIG. 1

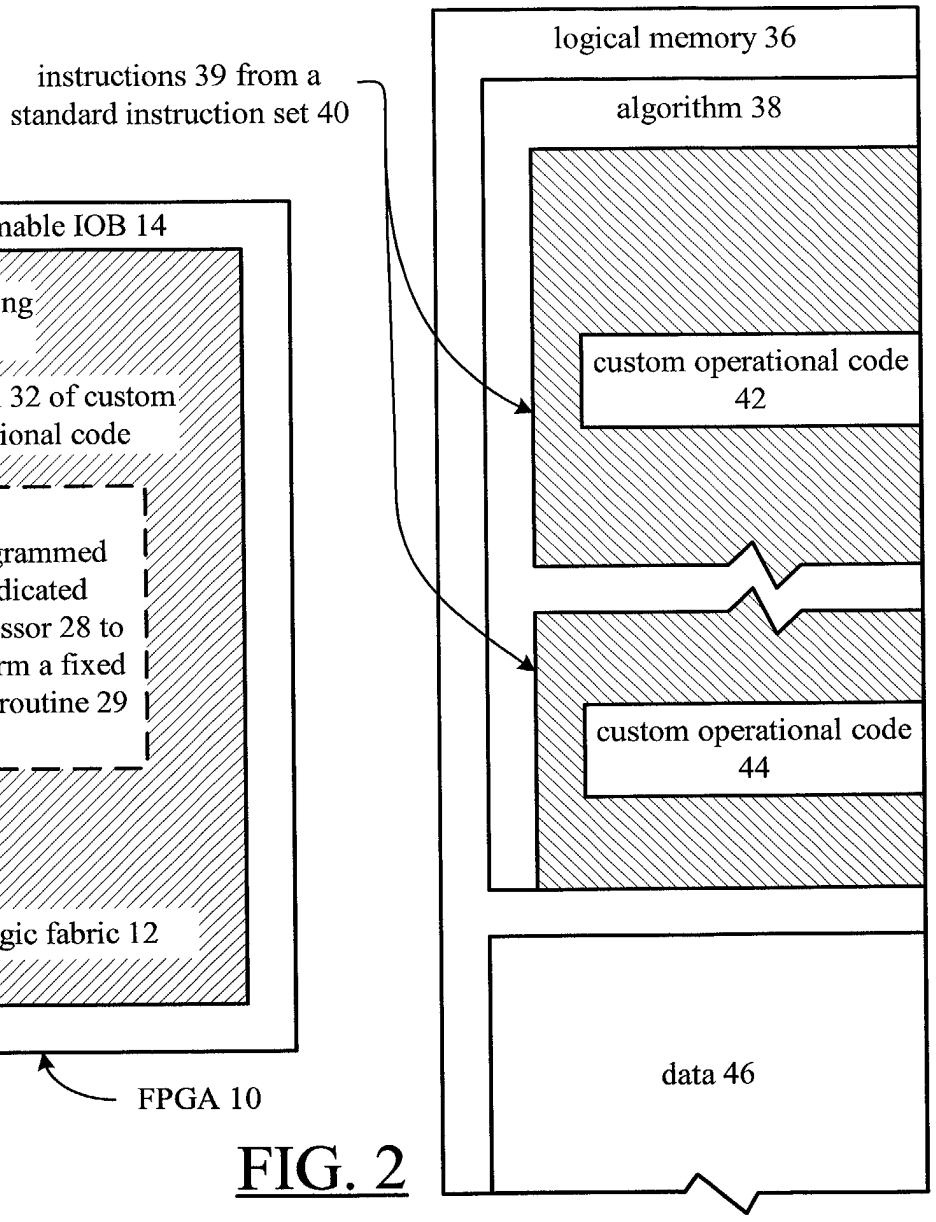
instructions 39 from a standard instruction set 40
logical memory 36
algorithm 38
custom operational code 42
custom operational code 44
data 46

FIG. 2

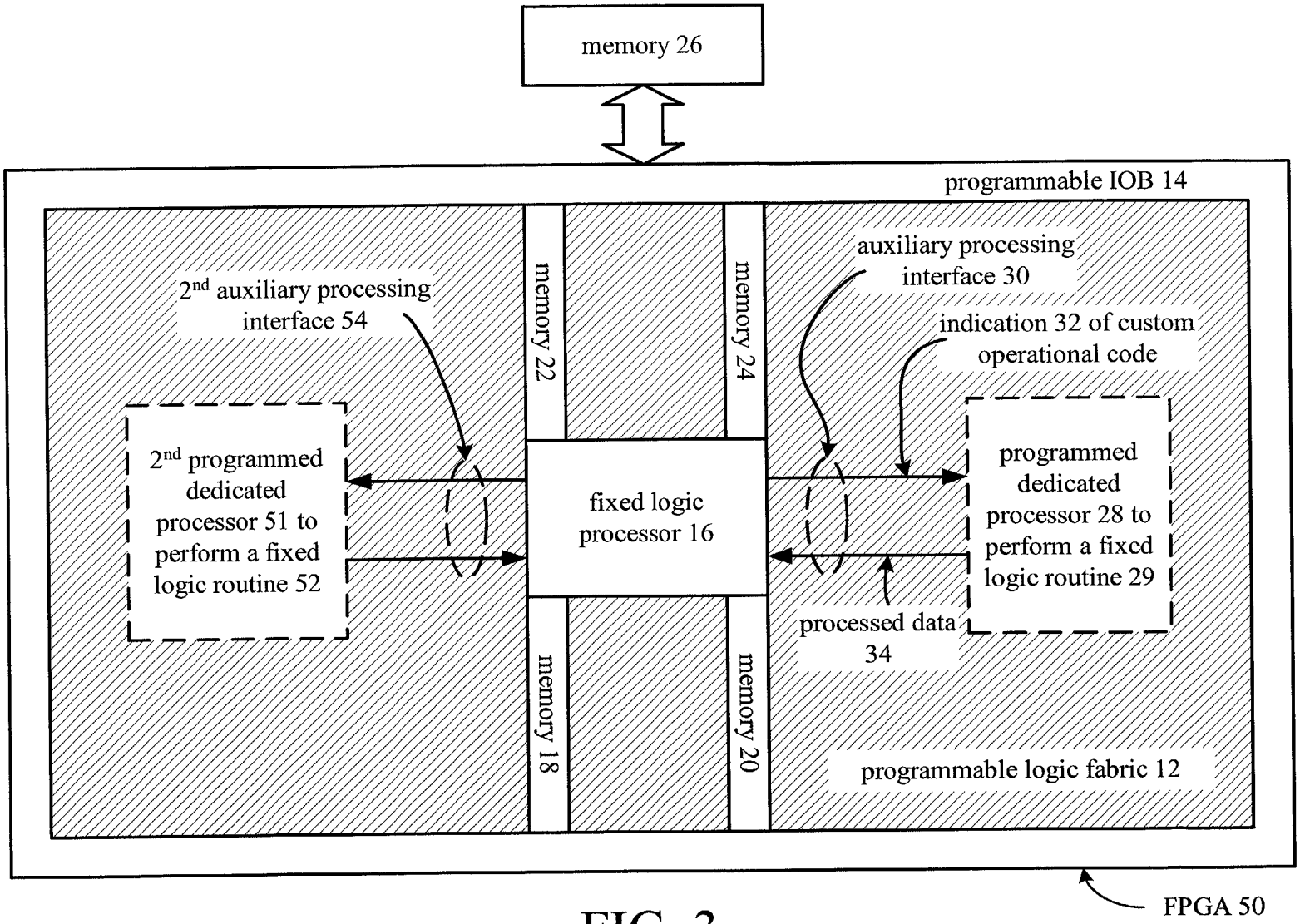

FIG. 3

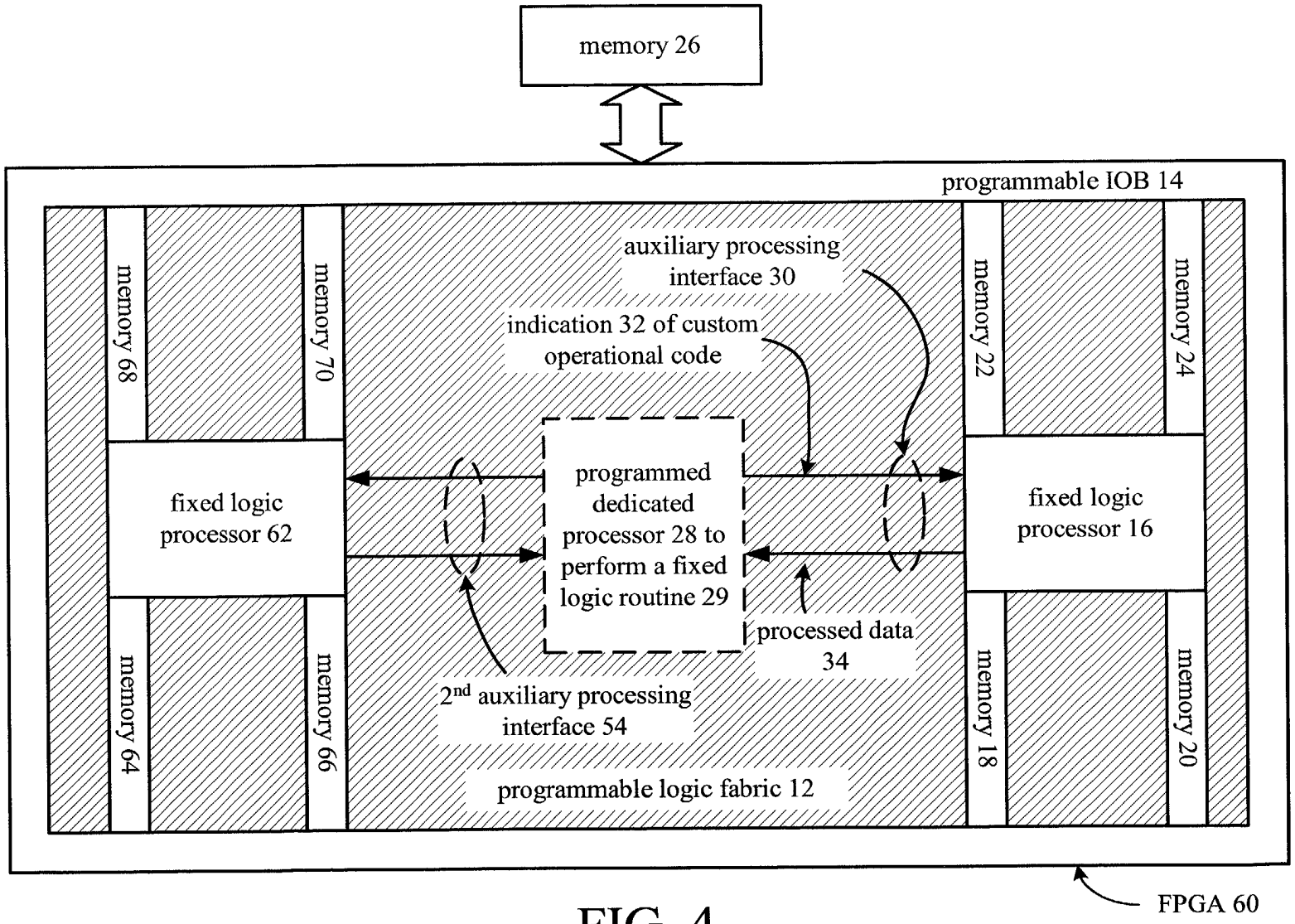
memory 26
programmable IOB 14
memory 68
memory 70
auxiliary processing interface 30
indication 32 of custom operational code
memory 22
memory 24
fixed logic processor 62
programmed dedicated processor 28 to perform a fixed logic routine 29
fixed logic processor 16
processed data 34
memory 64
memory 66
2nd auxiliary processing interface 54
memory 18
memory 20
programmable logic fabric 12
FPGA 60

FIG. 4

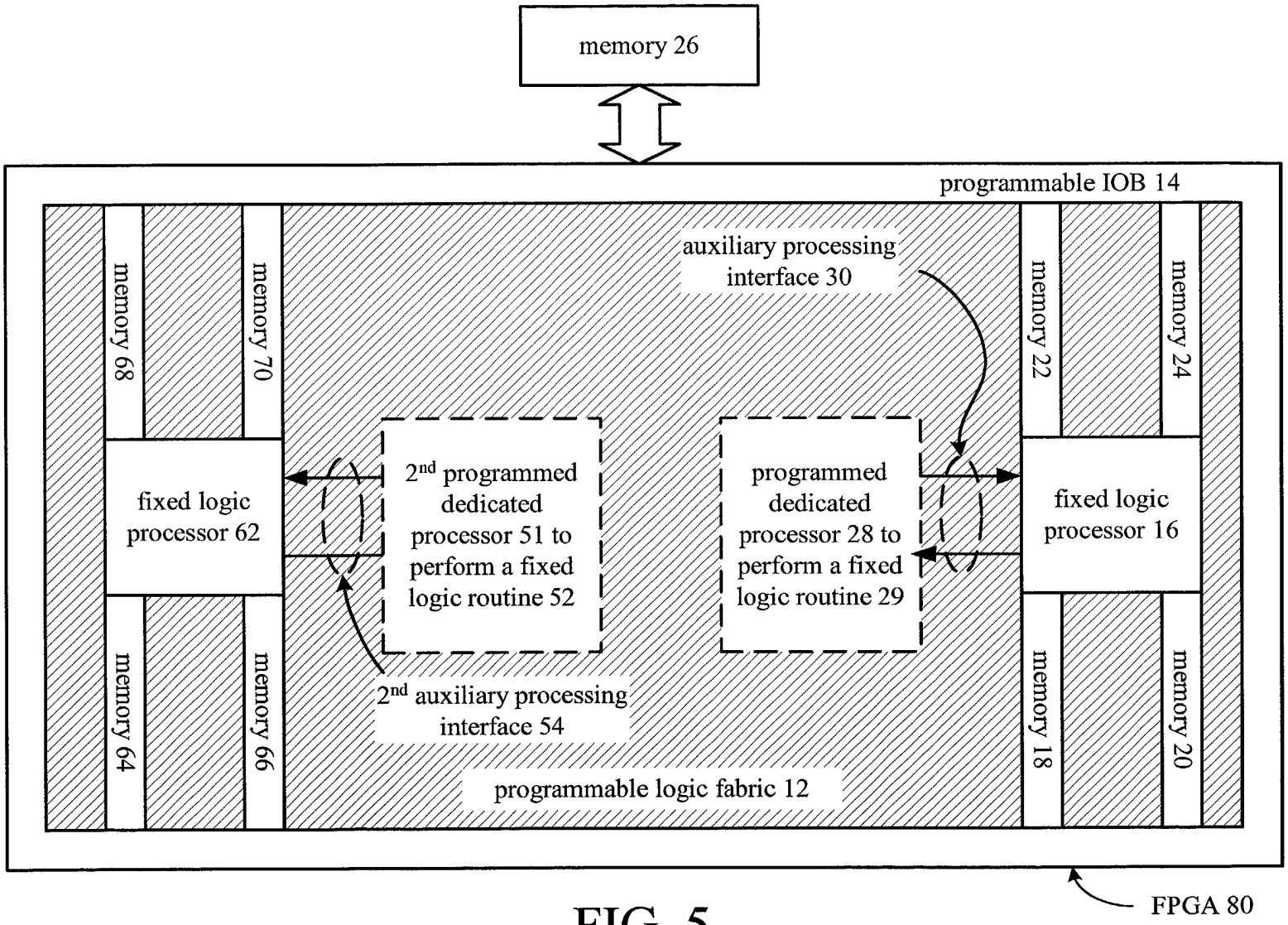
memory 26
programmable IOB 14
memory 68
memory 70
auxiliary processing interface 30
memory 22
memory 24
fixed logic processor 62
2nd programmed dedicated processor 51 to perform a fixed logic routine 52
programmed dedicated processor 28 to perform a fixed logic routine 29
fixed logic processor 16
memory 64
memory 66
2nd auxiliary processing interface 54
memory 18
memory 20
programmable logic fabric 12
FPGA 80

FIG. 5

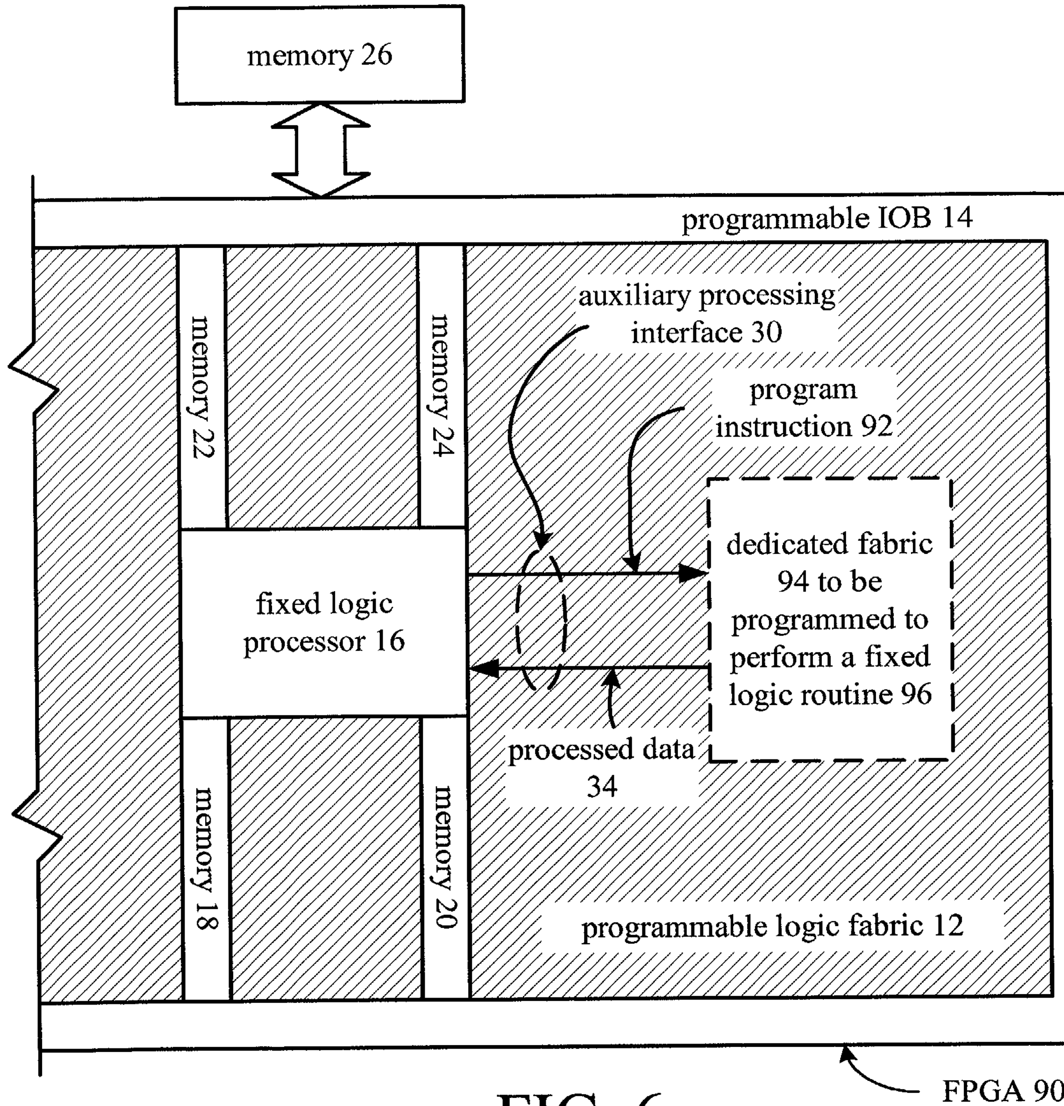
memory 26
programmable IOB 14
auxiliary processing interface 30
program instruction 92
dedicated fabric 94 to be programmed to perform a fixed logic routine 96
processed data 34
fixed logic processor 16
memory 22
memory 24
memory 18
memory 20
programmable logic fabric 12
FPGA 90

FIG. 6

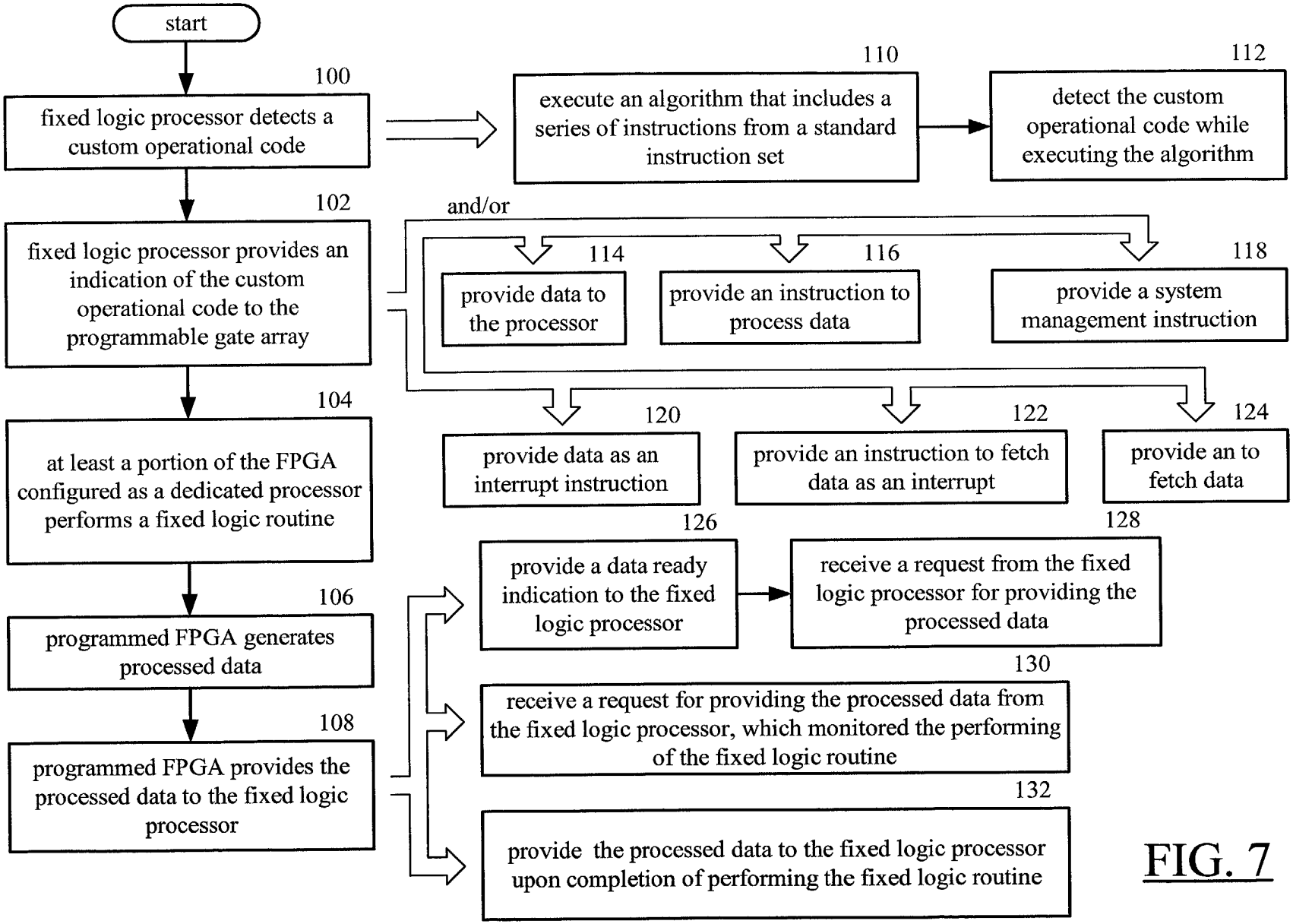
start
100
fixed logic processor detects a custom operational code
102
fixed logic processor provides an indication of the custom operational code to the programmable gate array
104
at least a portion of the FPGA configured as a dedicated processor performs a fixed logic routine
106
programmed FPGA generates processed data
108
programmed FPGA provides the processed data to the fixed logic processor
110
execute an algorithm that includes a series of instructions from a standard instruction set
112
detect the custom operational code while executing the algorithm
and/or
114
provide data to the processor
116
provide an instruction to process data
118
provide a system management instruction
120
provide data as an interrupt instruction
122
provide an instruction to fetch data as an interrupt
124
provide an to fetch data
126
provide a data ready indication to the fixed logic processor
128
receive a request from the fixed logic processor for providing the processed data
130
receive a request for providing the processed data from the fixed logic processor, which monitored the performing of the fixed logic routine
132
provide the processed data to the fixed logic processor upon completion of performing the fixed logic routine

FIG. 7

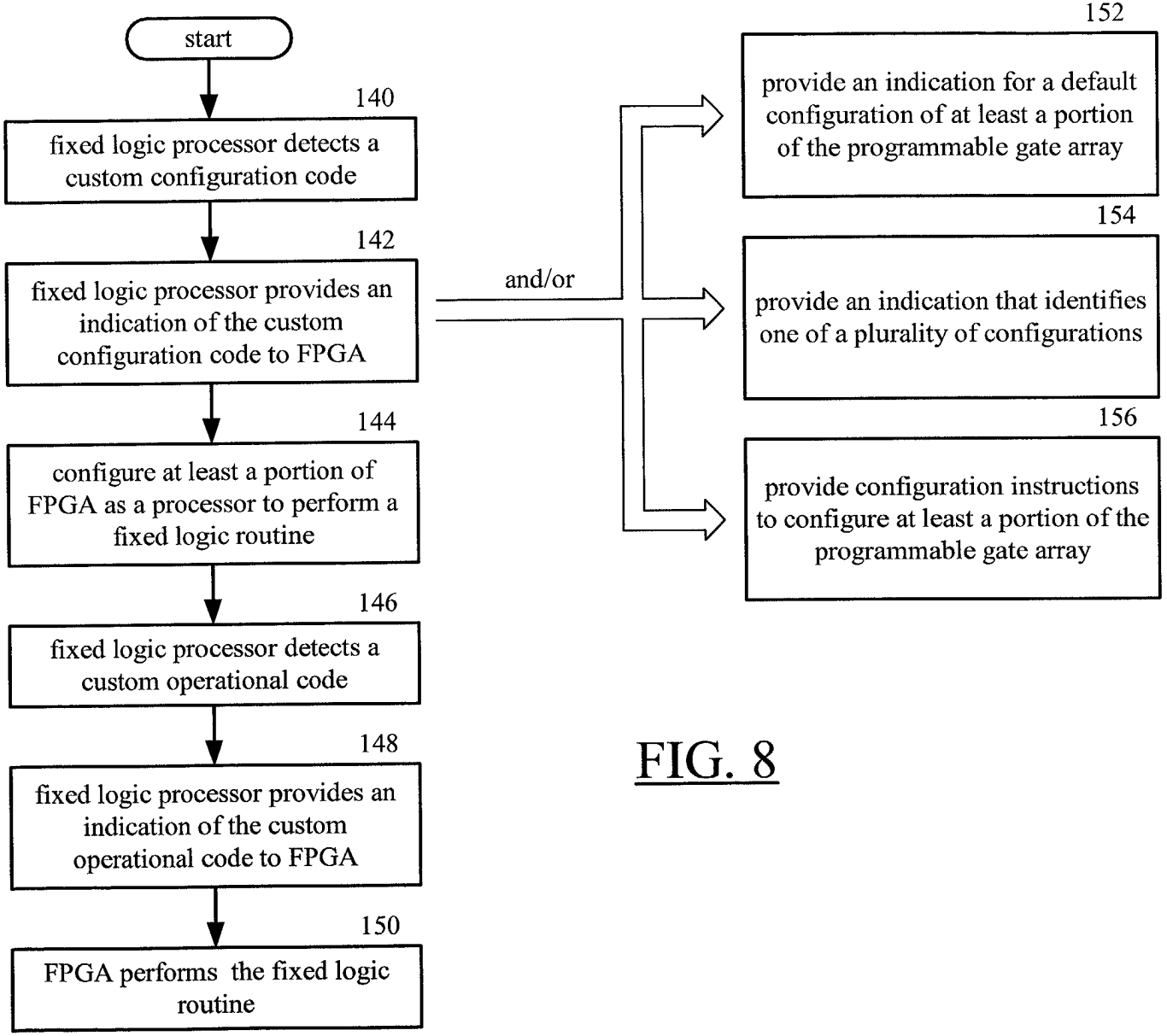
start
140
fixed logic processor detects a custom configuration code
142
fixed logic processor provides an indication of the custom configuration code to FPGA
144
configure at least a portion of FPGA as a processor to perform a fixed logic routine
146
fixed logic processor detects a custom operational code
148
fixed logic processor provides an indication of the custom operational code to FPGA
150
FPGA performs the fixed logic routine
and/or
152
provide an indication for a default configuration of at least a portion of the programmable gate array
154
provide an indication that identifies one of a plurality of configurations
156
provide configuration instructions to configure at least a portion of the programmable gate array

FIG. 8